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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,439	12/03/2003	Simon Lovett	2008.007100/02-0265	6743

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EXAMINER	
WENDLER, ERIC J	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,439	LOVETT, SIMON	
	Examiner	Art Unit	
	Eric Wendler	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/3/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on December 3, 2003.

2. Claims 1-56 are pending in the case. Claims 1, 15, 19, 30, 40, 45, 46, and 51 are independent claims.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "first transistor to provide a first input signal...wherein said transistor is an N-channel transistor" in claim 6 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. **Claims 46-50 are rejected** under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The details of the instruction code and how the code is executed to perform the method claimed in claims 46-50 are not sufficiently enabled in the specification so as to allow one skilled in the art to duplicate the writing of such instruction code which executes the process claimed.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-56 are rejected under 35 U.S.C. 102(b) as being anticipated by the US Patent to Yuh (6,154,408).

7. **Regarding claims 1-2, 11, 19, 26, 30, 36, 40-41, 45-47, and 51,** Yuh teaches a memory device comprising a circuit **10** (including leakage model circuit 21, Fig. 4) for performing an approximation of a current leakage associated with a portion of the

device. Yuh also teaches a refresh rate control unit **14**, **16**, operatively coupled with circuit **10**, comprising a refresh oscillator, to adjust a refresh rate associated with at least a portion of the device in response to an approximation of current leakage (Abstract; and column 2, lines 3-23).

8. **Regarding claims 3, 20, 31, 53, and 56,** Yuh teaches that the memory device is a DRAM (column 1, lines 14-18). It is inherent that a DRAM comprises at least one memory cell.

9. **Regarding claims 4, 15, 22, 32, and 55,** Yuh teaches a transistors **MP21, MP22**, to provide an input signal **wr**; a cell leakage model **21** operatively coupled to the transistor, to model a current leakage associated with a portion of the device; a comparator **12** to compare the input signal to a reference input signal; and a delay unit **45** operative coupled to the comparator to provide a delay upon an output from the comparator to provide a time period for pre-charging of the transistor and provide a signal for controlling the refresh rate, and a refresh control oscillator operatively coupled to the delay unit to provide the refresh rate signal **osc** or refreshing at least a portion of the memory device.

10. **Regarding claims 5, 6, 23, and 33,** Yuh teaches that the transistor is a P-channel transistor. The open language (use of "here" implies that P-channel transistors are used in this instance, but other types of transistors can be used as well) of the teachings of Yuh suggests that other types of transistors, such as N-channel transistors, which are well known in the art, can also be used (column 3, lines 50-51).

11. **Regarding claim 7,** Yuh teaches that the current leakage model **21** comprises a second transistor **MN11** for modeling the current leakage of at least a portion of the device.

12. **Regarding claims 8, 9, 24, and 34,** Yuh teaches that the comparator 12 comprises a differential amplifier **35** and CMOS inverters.

13. **Regarding claims 10, 25, and 35,** Yuh teaches that the delay unit comprises a plurality of inverters wherein each of the inverters provides a delay (Fig. 8).

14. **Regarding claims 12, 16, 27, 37, 42, and 48,** Yuh teaches that the circuit is capable of modeling a leakage current that is induced by a temperature level (column 1, lines 62-67).

15. **Regarding claims 13-14, 17-18, 28-29, 38-39, 43-44, and 49-50,** it is inherent that operating voltage levels and particular process features induce current leakage. Whenever operating voltages or processes of memory, such as writing, are used, it is inherent that there will be induced current leakage. Yuh teaches that his circuit is capable of modeling current leakage, which would encompass these types of inherent current leakage involved with memory.

16. **Regarding claims 19, 21, 46, 51, 52, and 54,** Yuh teaches that his device can be used in a notebook personal computer, which contains a system board which is a motherboard of a computer system, a processor, a computer readable program storage device encoded with instructions that can be executed to perform a method, and a display device, which is a monitor, coupled to a computer unit with a system board.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fiscus (US 2002/0196692) teaches circuit which is configured to vary a refresh rate of a memory cell in response to changes in temperature.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Wendler whose telephone number is (571) 272-5063. The examiner can normally be reached on Monday - Friday 8AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJW
2/28/06

Tuan T. Nguyen
3/4/06